Data Acquisition and Trigger Upgrades

Jamie Nagle
Columbia University

RHIC Detector Workshop:
R&D for Future Detectors and Upgrades
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Brookhaven National Laboratory

Outline

- How the physics drives the DAQ/Trigger requirements?
- How to trigger on rare physics at higher luminosities?

  High Level Triggers for Heavy Ions
  Level-1 Triggers for proton spin program

- How to deal with much larger data volume detectors?

  Large archiving rates
  New data compression schemes
  Reconstruction Farms and online DST production

- How to make this a reality on the right time scale?

Must be Driven by the Physics

RHIC II must compete with / complement LHC Heavy Ion Physics

Polarized p-p, p-A and eventually e-A are unique opportunities

What physics needs higher luminosity?

- γ-jet physics (eg. minor Trigger change in PHENIX)
- Υ physics

What physics needs new detectors with large data volume?

- low mass vector mesons (silicon, TPC, HBD)
- open charm (silicon, compact TPC)

Spin Physics will have very different DAQ/Trigger requirements

New Detector for p-A, e-A would have new requirements

LHC Example

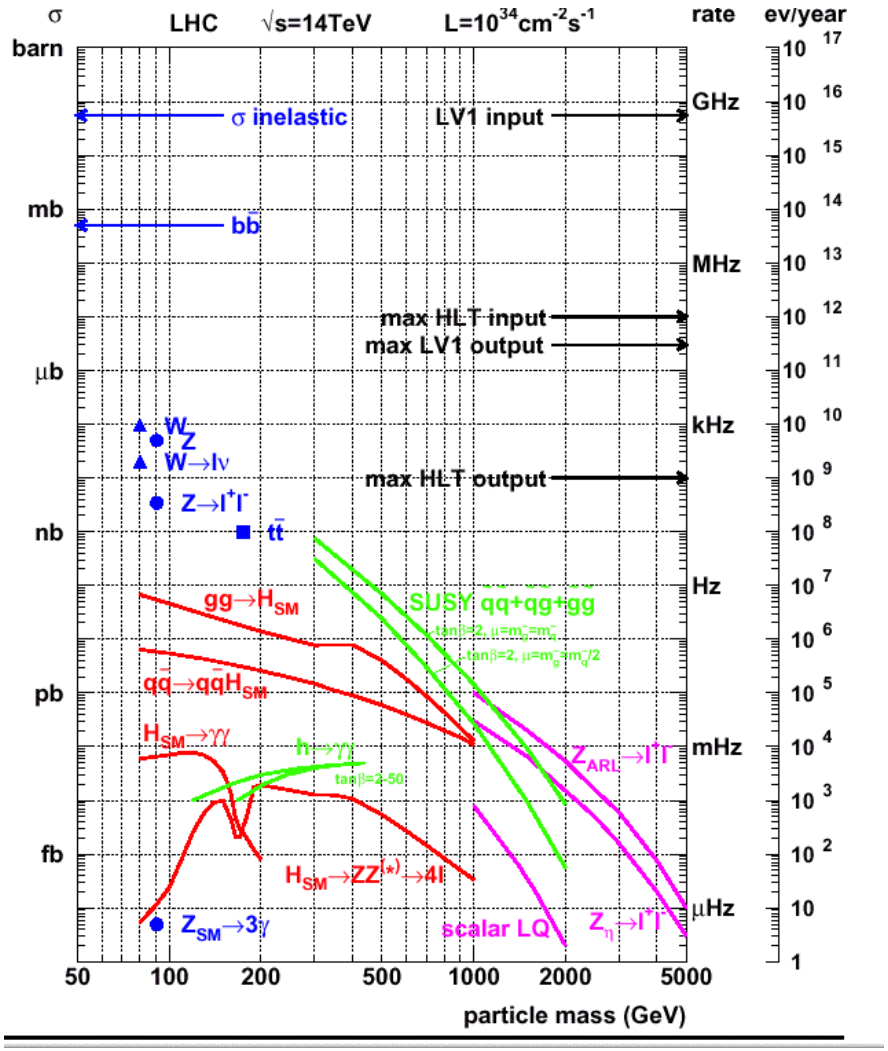
LHC design

~1 GHz input rate
~1 kHz W events
~10 Hz top events
<<< 1 Hz Higgs events

Can store ~ 100 Hz

Level-1 Triggers
1 GHz ‡ 100 kHz
High Level Triggers
100 kHz ‡ 100 Hz

The picture at RHIC is not as clear. Many different physics signatures spanning a very full range.



RHIC Luminosities

Heavy Ions:

	RDM	RDM+	RHIC II	
Peak Luminosity, L_0	0.8	3.2	8.3	[10^{27} cm^{-2}s^{-1}]
	5.6	20.0	**49.0**	[AuAu min. bias **kHz**]

•10 hour store for RDM and RDM+, and 5 hour store for RHIC II
• RDM+ assumes beta* = 1 m and 112 bunches
• RHIC II assumes electron cooling to reduce emittance and counteract IBS

Proton-Proton:

	RDM	RDM+	RHIC II	RHIC II++	
Peak Luminosity, L_0	1.5	24.0	40.0	400.0	[10^{31} cm^{-2}s^{-1}]
	0.6	9.6	**24.0**	**240.0**	[pp **MHz**]

• RMD+ assumes only collisions at 3 IR's
• RHIC II assumes only collisions at 2 IR's

Changing 9.4 MHz frequency

Important impact on possible new experiment

New Detector Challenges

Large data volume
eg. Currently
PHENIX ≡ 400 kB/evt (cent)
STAR ≡ 8 MB/evt (cent)

Silicon Detectors:

PHENIX: Barrel pixels ≡ 7.8 million channels
Barrel strips ≡ 0.5 million channels
Endcap pixels ≡ 94.0 million channels
raw data volume **200 kBytes** (zero supp)
assumes very low noise

STAR: Vertex Upgrade ≡ 90.0 million channels
Forward Disks ≡ 0.6 million channels
Silicon Drift ≡ 3.4 million channels (**10 Mbytes**)

PHOBOS: Vertex detector ≡ 0.1 million channels

New TPC:

Possible Level-1 Trigger Detectors
Very Challenging in Busy Environment

STAR/PHENIX:

TPC compact – 80 k channels
16 Mbytes ≡ **0.8 Mbytes** (zero supp)

Data Flow

Data Link to Readout Buffers

Optical Technology

Level-1 Triggers

High Density FPGA, Custom ASIC (?)

Data Processsing and Transfer

Custom Electronics, Bus Speed

Level-2 Hardware Triggers

Trigger Primitive Processors

Event Building Switch

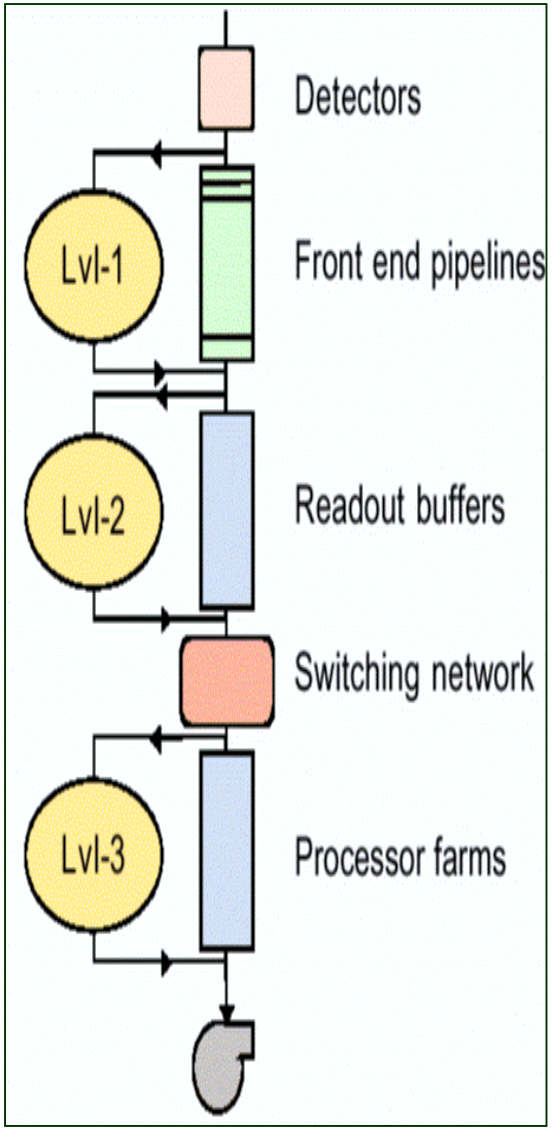
Gigabit Ethernet++, ATM

Level-3 Processor Farms

Operating System, Number of Nodes, Software

Data Archiving

Tape Cost, Storage Technology, Ability to Analyze



Level-1 Triggers

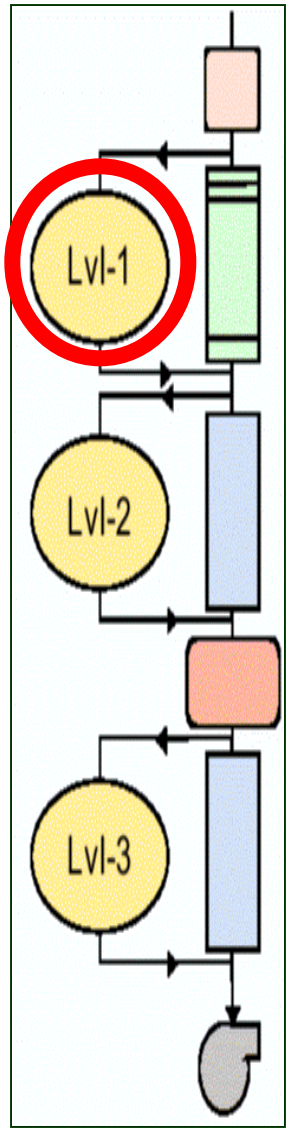
Custom electronics for fast trigger selection

- Typical Level-1 trigger latency 2-4 microseconds
- Fully pipelined FPGA systems
- Really pushing the technology limit of FPGA's
- Possibly necessitate custom ASIC development

Current Maximum Level-1 Rate

PHENIX Lvl1 Rate = 12.5 kHz
Simple $2 M Upgrade = 25.0 kHz
Beyond that one needs to replace all
existing Front-End Electronics ~ $30 M

STAR Lvl1 Rate = 100 Hz
Need to Replace TPC Electronics or TPC



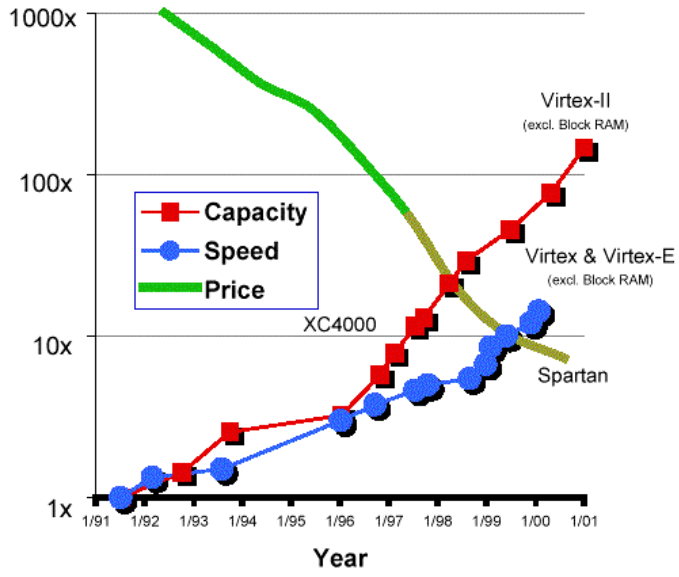
Level-1 Triggers

Very close coordination between Front-End Electronics and Level-1 Trigger development is required.

FPGA Technology is changing very fast. RHIC community must keep up to date in order to design and produce electronics in the future.

Required R&D Funding

Focus on Level-1 for muons, calorimeters, and possible silicon detectors. So far at RHIC there are no custom ASIC's for Level-1 Triggers. That is a key threshold in terms of R&D and total manpower.



LHC R&D Projects

Research & Development Projects

RD12

Timing, Trigger and Control Systems for LHC Detectors

RD24

Application of the Scalable Coherent Interface (SCI) to Data Acquisition at LHC.

RD27

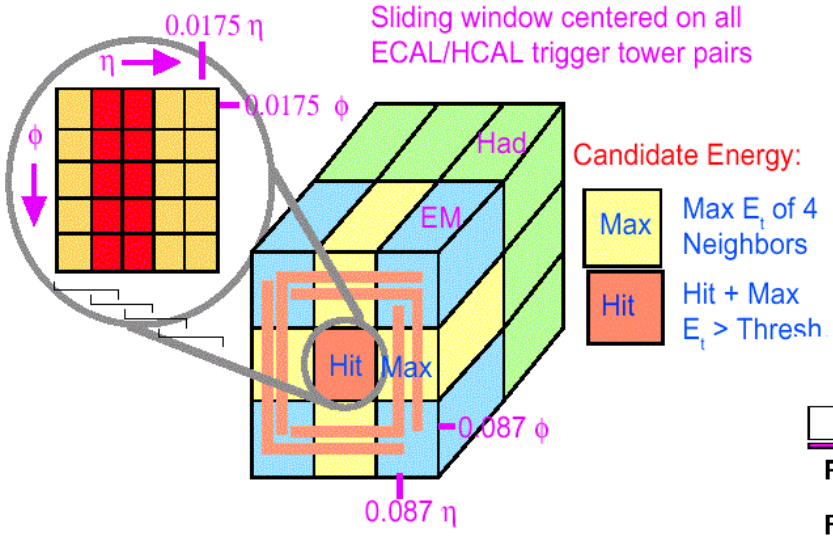
Study of first-level trigger systems for general-purpose LHC experiments.
Goal to develop demonstrators for fast optical links, fast electronic data transmissions between boards and crates, fast high-density FPGA, muon Level-1 trigger with coincidence matrix ASIC

RD31

Application of ATM to data acquisition for High Energy Physics

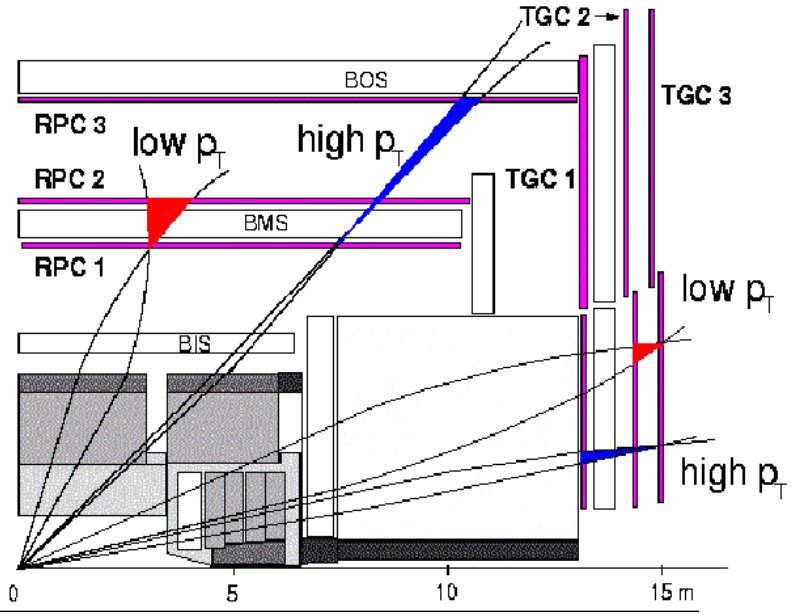
- Projects started in the early 90's for LHC program.
- Overall scale (eg. manpower) much larger than available for RHIC upgrades
- Some success, in particular TTC from RD12

ASIC Development at LHC



CMS Calorimeter Regional Trigger Electron Isolation ASIC: 160 MHz 0.6 μm high-integration GaAs custom gate array

ATLAS Muon Trigger high & low p_t coincidence logic in 0.6 μm and 0.35 μm CMOS full-custom ASICs



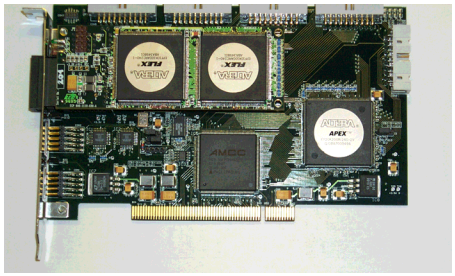
Data Transfer / Processing

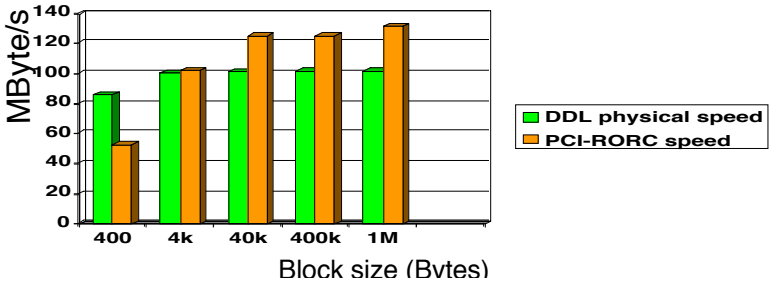
Data transferred from Front-End Electronics to Data Collection Boards

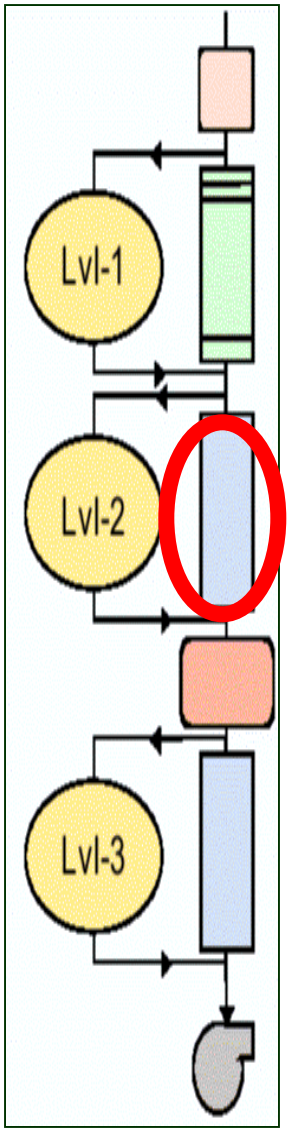
- Early RHIC R&D on Optical Technology
- Important R&D to keep up with increasing speed

Data transfer into Processors

- Faster Digital Signal Processors for Custom Boards versus Cost Performance of PC
- Custom electronics in VME
  - (eg. PHENIX – custom bus 160 MB/s)
- Direct into PCI bus
  - (eg. PHENIX jSEB - ~ 40 MB/s)
  - (eg. ALICE PCI-RORC – goal ~ 100 MB/s)

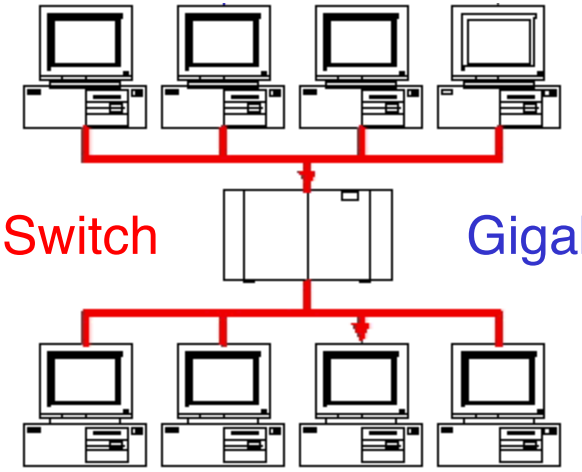




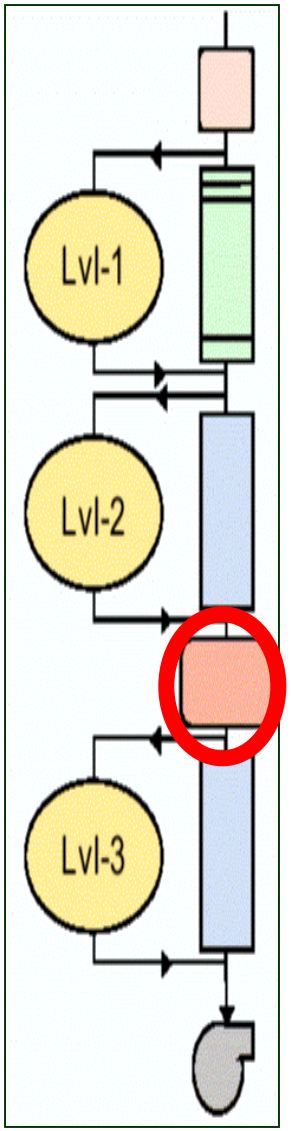


Event Building

Common model is to accumulate data segments in PC's and then build events into more PC's across a switch.



PHENIX currently uses ATM.
RD31 at CERN investigated ATM. None of LHC experiments will use ATM.
Gigabit Ethernet prices are dropping. Gigabit++.

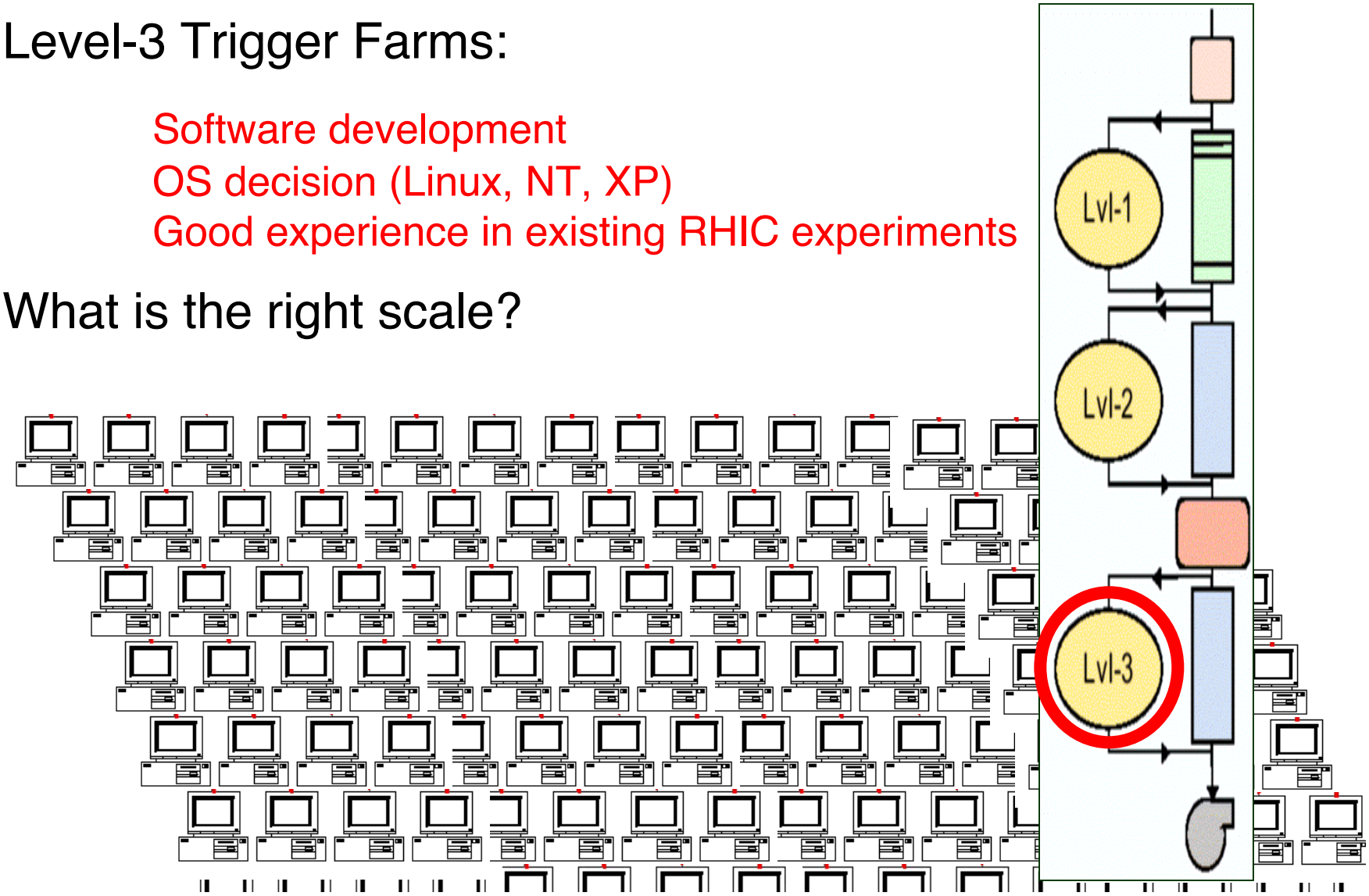


High Level Triggers

Level-3 Trigger Farms:

Software development
OS decision (Linux, NT, XP)
Good experience in existing RHIC experiments

What is the right scale?



Data Archiving

PHENIX+STAR ~20 MB/s

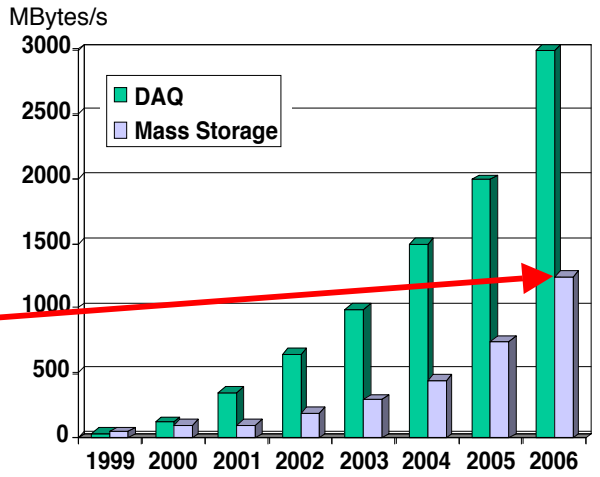
ATLAS + CMS ~100 MB/s

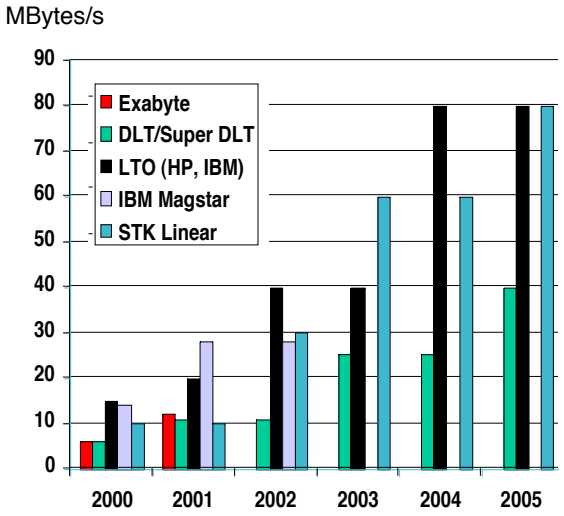
ALICE ~1250 MB/s

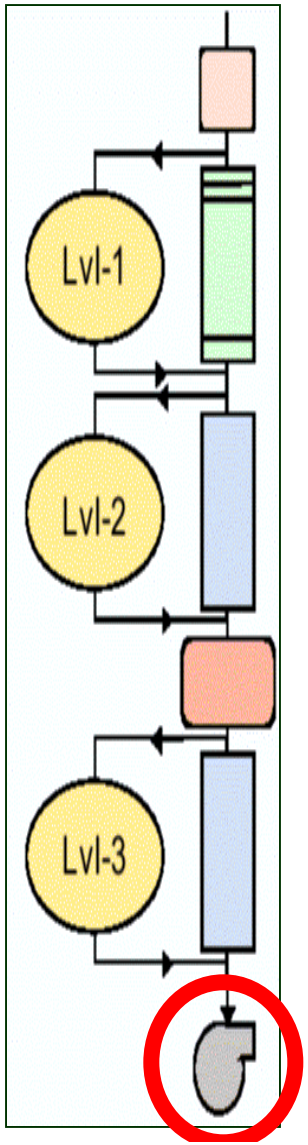
- Centrality trigger only for central detector
- Muon readout done separately
- Key factor ≠ short runs

Probably not a good option for RHIC II with 30 weeks/year

However 100 MB/s might be reasonable







Lessons from ALICE

Event size ~ 30 MB (0.25 MB)

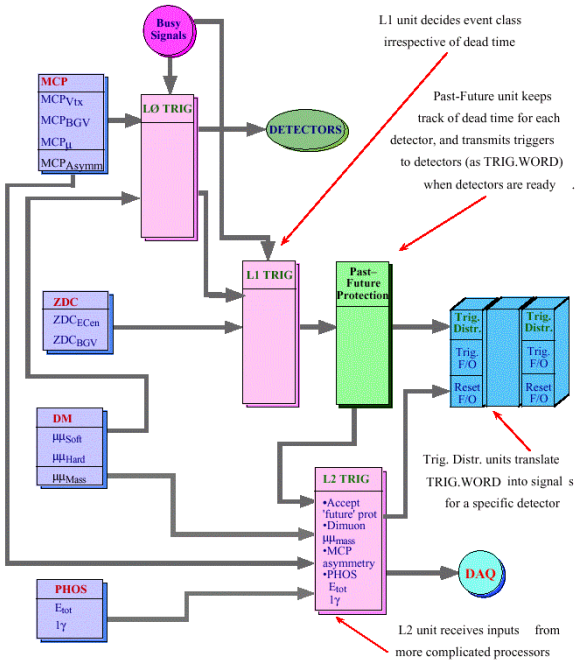
Level-1 Trigger Rate ~ 1 kHz

Archiving Rate ~ 100 Hz (1 kHz)
~ 1.25 Gigabytes/s

ALICE has split DAQ Readout !

Only centrality trigger for central detector

Dimuon trigger for separate readout



Already they are working on how to have more Level-1 triggers to enhance open charm for example.

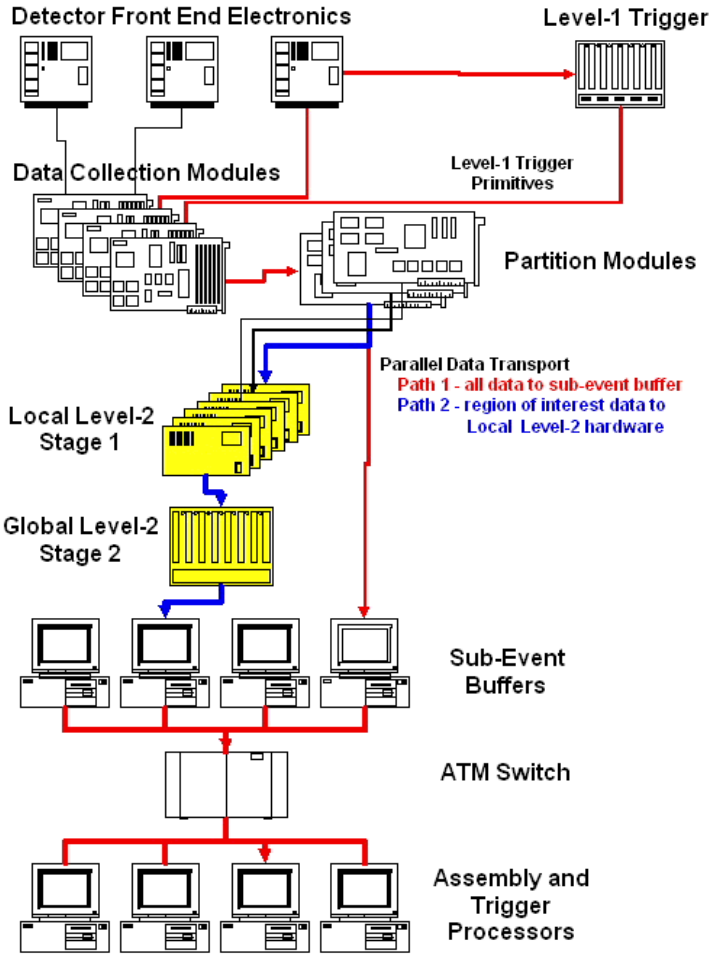
My Example

PHENIX is upgrading the High Level Trigger system for Run 3 with a Region of Interest Trigger Pre-Processor for Muons, EMCal.

Custom electronics with cutting edge DSP and FPGA technology.

DSP (beta version of TI 400 MHz) 10x faster than DSP currently used

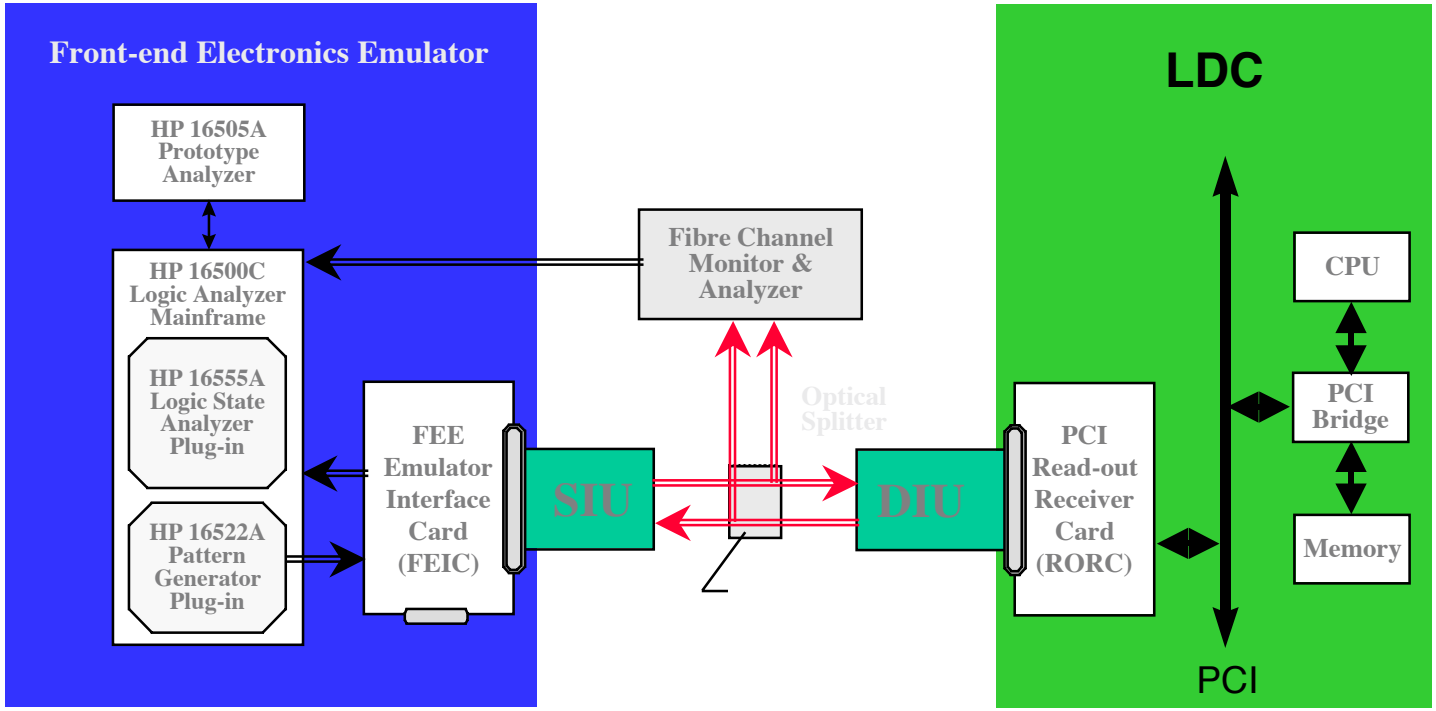
Investment of $150k for DOE-OJI allows Nevis Laboratories to keep current of technology that is required for RHIC II upgrades.



Equipment for Testing

Test equipment and early prototypes for demonstration projects will be necessary. Development cycle is at least 2-3 years for new optical, FPGA, DSP technology.

Test setup for ALICE FEE to LDC prototype



R & D Funding

Early RHIC R&D Funding

There was a RHIC R&D program, associated with the RHIC Project, with about $15M for detector R&D over the period FY 90 - FY 95.

The early funding was "generic R&D", and we had an advisory committee to help us respond to proposals.

A major focus was on custom IC development. We saw this to be a critical issue in developing detectors with the huge number of channels needed for RHIC physics. Even though analog pipeline technology existed back then, we felt there was a ~6 year development effort before one could start producing chips that were specific for RHIC detectors. Development efforts were funded at BNL, LBNL, ORNL, Columbia, and MIT. These were each at the level of about $100K/year for the first 3 years. As the detector collaborations and conceptual designs emerged, the R&D funding became more detector-specific, but the funding for chip development at these institutions remained at about this same level.

Similar program for R&D is needed for next 2-3 years on Trigger Electronics (FPGA, DSP, Custom ASIC), Optical, Data Bus, Network Switching, and more to be seen in this workshop….

Pre-Workshop Summary

Triggers:

Fast DSP and FPGA technology must be studied
Major effort for silicon based level-1 triggers
Question on whether custom ASIC's are necessary

Data Acquisition:

Data compression and Processing
Data Bus Transfer
Network Switching

It was a large challenge to develop collider electronics experts for RHIC, and an equal technology challenge exists for RHIC II.

Many contributions from:
Pierre Vande Vyvre
Cheng-Yi Chi
Paris Sphicas
Tonko Ljubicic
and many more